# PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2001-308152
(43)Date of publication of application : 02.11.2001

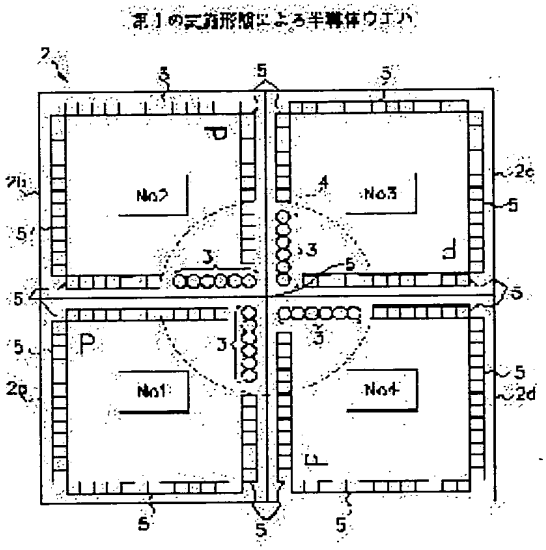
(51)Int.Cl. H01L 21/66
G01R 1/06
H01L 21/60

(21)Application number : 2000-120372
(22)Date of filing : 21.04.2000

(71)Applicant : FUJITSU LTD
(72)Inventor : UI NOBUYUKI
HYODO MASATO

## (54) SEMICONDUCTOR WAFER AND ITS TESTING METHOD

(57)Abstract:
PROBLEM TO BE SOLVED: To shorten a manufacturing time and delivery time of a semiconductor chip by a method wherein the same probe card is shared when the semiconductor wafer is tested irrespective of a semiconductor chip size.
SOLUTION: Semiconductor chip regions 2a to 2d of a plurality of polygons are mutually adjacent to each other on a semiconductor wafer. Each semiconductor chip region is provided with a testing bonding pad 3 in at least any side out of the sides of the polygons adjacent to each other, respectively. A probe card needle is simultaneously brought into contact with a testing bonding pad of the plurality of semiconductor chip regions adjacent to each other, and normalities or abnormalities of the plurality of semiconductor chip region are simultaneously tested. Even when the semiconductor chip size changes, the testing bonding pad within the semiconductor chip region can be disposed at the same position and the same probe card can be shared when the semiconductor wafer is tested.




LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

**Japanese Patent Publication Laid-Open No. 2001-308152**



[Claim(s)]

[Claim(s)]

[Claim 1] It is the semi-conductor wafer characterized by the thing of the sides which it is the semi-conductor wafer which has the group of the semiconductor chip field of the multipolygon which adjoins mutually, and each semiconductor chip field adjoins mutually within the group of said semiconductor chip field, respectively for which one of the sides was equipped with the bonding pad for a trial at least.

[Claim 2] Each semiconductor chip field is a semi-conductor wafer according to claim 1 characterized by the thing of the sides of said polygon which adjoins mutually for which one of the sides was equipped with the bonding pad for a trial at least, respectively including the semiconductor chip field of the polygon of four pieces where said semi-conductor wafer adjoined mutually.

[Claim 3] Each semiconductor chip field is a semi-conductor wafer according to claim 1 characterized by the thing of the sides of said polygon which adjoins mutually for which one of the sides was equipped with the bonding pad for a trial at least, respectively including the semiconductor chip field of the polygon of three pieces where said semi-conductor wafer adjoined mutually.

[Claim 4] It is the semi-conductor wafer which has the group of the semiconductor chip field of the multipolygon which adjoins mutually. Each semiconductor chip field is the test method of the semi-conductor wafer of the sides which adjoin mutually within the group of said semiconductor chip field, respectively which equipped one of the sides with the bonding pad for a trial at least. The test method of the semi-conductor wafer which a probe card needle is simultaneously contacted to the bonding pad for a trial of two or more of said semiconductor chip fields which adjoin mutually, and examines simultaneously two or more of said normal or abnormalities of a semiconductor chip field which adjoin mutually.

[Claim 5] Said semi-conductor wafer includes the semiconductor chip field of the polygon of four pieces which adjoined mutually. Each semiconductor chip field It is the test method of the semi-conductor wafer of the sides of said polygon which adjoins mutually which equipped one of the sides with the bonding pad for a trial at least, respectively. The test method of the semi-conductor wafer according to claim 4 which a probe card needle is simultaneously contacted to the bonding pad for a trial of said four semiconductor chip fields which adjoin mutually, and examines simultaneously said normal or abnormalities of four semiconductor chip fields which adjoin mutually.

[Claim 6] Said semi-conductor wafer includes the semiconductor chip field of the polygon of three pieces which adjoined mutually. Each semiconductor chip field It is the test method of the semi-conductor wafer of the sides of said polygon which adjoins mutually which equipped one of the sides with the bonding pad for a trial at least, respectively. The test method of the semi-conductor wafer according to claim 4 which a probe card needle is simultaneously contacted to the bonding pad for a trial of said three semiconductor chip fields

which adjoin mutually, and examines simultaneously said normal or abnormalities of three semiconductor chip fields which adjoin mutually.

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to the semi-conductor wafer suitable for examining simultaneously two or more semiconductor chip fields especially on a semi-conductor wafer, and its test method about a semi-conductor wafer and its test method.

[0002]

[Description of the Prior Art] Drawing 9 shows the measuring method in the semi-conductor wafer trial by the conventional technique. Two or more semiconductor chip fields 52 of four square shapes are formed on the semi-conductor wafer. A bonding pad (henceforth a pad) 55 is formed on four sides of the semiconductor chip field 52. The power-source pad 57 is formed as some pads 55.

[0003] In order to examine this semiconductor chip field 52, a probe card 54 is used. A probe card 54 has the probe card needle 56 of the number of pads 55, and the same number. Each needle of the probe card needle 56 is contacted to each pad of a pad 55, respectively, and the normal or the abnormalities of the semiconductor chip field 52 are examined.

[0004] In this case, when examining other semiconductor chip fields on a semi-conductor wafer, it examines by moving a probe card 52 on other semiconductor chip fields. Therefore, only one semiconductor chip field 52 can examine by one trial.

[0005]

[Problem(s) to be Solved by the Invention] Since the degree of integration of the component manufactured on a semi-conductor wafer is improving while the aperture of a semi-conductor wafer increases in recent years, the number of semiconductor chips generated from the semi-conductor wafer which is is increasing rapidly. Therefore, the time amount which examines all the semiconductor chip fields on a semi-conductor wafer is huge. In order to shorten the test time of a semi-conductor wafer, how to show two or more semiconductor chip fields on a semi-conductor wafer in the following measured simultaneously can be considered.

[0006] Drawing 10 shows the coincidence measurement approach of two or more semiconductor chip fields which can be set to a semi-conductor wafer trial. How to measure simultaneously four semiconductor chip fields 62 which adjoin on a semi-conductor wafer is shown. Each semiconductor chip field 62 has the pad 63 for a trial in left part, and has a pad 65 the right-hand side, a top chord, and the lower side. The pad 63 for a trial is a pad used also in a semi-conductor wafer trial, and it not only uses it at the time of normal operation, but it contains a power-source pad.

[0007] Although examined by contacting the probe card needle 56 to all the pads 55 in the test method shown in drawing 9 , if the probe card needle 66 is contacted only to the pad 63 for a trial of drawing 10 according to the scanning (SCAN) design technique and it examines, normal or abnormalities, such as a component in the semiconductor chip field 62 or connection, can be investigated.

[0008] A probe card 64 has the probe card needle 66 of the number of the pads 63 for a trial of four semiconductor chip fields 62, and the same number. Each needle of the probe card needle 66 can be contacted to each pad of the pad 63 for a trial, respectively, and the normal or the abnormalities of four semiconductor chip fields 62 can be examined simultaneously. According to this coincidence measurement approach, since four semiconductor chip fields 62 can be measured simultaneously, semi-conductor wafer

test time can be shortened.

[0009] This probe card 64 has the probe card needle 66 according to the location of the pad 63 for a trial of the semiconductor chip field 62. When the magnitude of the semiconductor chip field 62 changes, the location of the pad 63 for a trial and die-length LL between each pad 63 for a trial also change, and it must stop for this reason, newly having to create another probe card 64. whenever [ which designs a new semiconductor chip actually since a semiconductor chip is in the inclination of the formation of many forms ] -- a semi-conductor chip size -- changing -- the location of the pad 63 for a trial -- not changing -- it is necessary to obtain but to create the new probe card 64

[0010] In recent years, especially in the system ASIC, want of a short delivery date has become strong. Moreover, turn around time is becoming short by improvement in a semi-conductor design and a process technique. Therefore, the time amount required in order to newly create a probe card 64 is the main factors of the delay of a delivery date, and it is expected that the inclination becomes strong further from now on.

[0011] No matter this invention may be what semi-conductor chip size, by sharing a probe card at the time of a semi-conductor wafer trial, it abolishes the need of newly creating a probe card, and aims at attaining reduction-ization of cost in the production time of a semiconductor chip, and the shortening list of a delivery date.

[0012]

[Means for Solving the Problem] The test method of the semi-conductor wafer of this invention is a semi-conductor wafer which has the group of the semiconductor chip field of the multipolygon which adjoins mutually, and each semiconductor chip field examines using the semi-conductor wafer of the sides which adjoin mutually within the group of a semiconductor chip field, respectively which equipped one of the sides with the bonding pad for a trial at least. In that case, a probe card needle is simultaneously contacted to the bonding pad for a trial of two or more semiconductor chip fields which adjoin mutually, and two or more normal or abnormalities of a semiconductor chip field which adjoin mutually are examined simultaneously.

[0013] Since this invention consists of the above-mentioned technical means, the bonding pads for a trial of each semiconductor chip field gather near the central point the semiconductor chip field of a multipolygon adjoins mutually. Even when the size of a semiconductor chip changes by collecting the bonding pads for a trial, it becomes possible to arrange the bonding pad for a trial in the same location. If the location of BONTINGUPADDO for a trial is decided without depending on the size of a semiconductor chip, it will become unnecessary to be able to share the probe card same at the time of a semi-conductor wafer trial, and to newly create a probe card according to the semiconductor chip of different size.

[0014]

[Embodiment of the Invention] Hereafter, the operation gestalt of this invention is explained based on a drawing.

(1st operation gestalt) Drawing 1 is the top view of the semi-conductor wafer by the 1st operation gestalt of this invention. The semiconductor chip field unit 2 is constituted using semiconductor chip field 2a of four square shapes [ four ], 2b, and 2c and 2d as 1 set. As shown in drawing 2 , two or more arrays of the semiconductor chip field unit 2 are carried out on the semi-conductor wafer 1.

[0015] drawing 1 -- setting -- semiconductor chip field 2a and 2b of four pieces, and 2c and 2d -- this -- four semiconductor chip fields 2 -- a-2d is the same pattern as the pattern each other rotated by a unit of 90 degrees on the flat surface of a semi-conductor wafer centering on the central point (adjacent point) 6 which

touches mutually, respectively. The pattern on each semiconductor chip field 2a, 2b, 2c, and 2d "P" is to show semiconductor chip field 2a, 2b, and the sense of each pattern (2c and 2d).

[0016] Specifically, upper left semiconductor chip field 2b is the same pattern as the pattern made to rotate clockwise lower left semiconductor chip field 2a 90 degrees on the flat surface of a semi-conductor wafer centering on a point 6. Upper right semiconductor chip field 2c is the same pattern as the pattern made to rotate upper left semiconductor chip field 2b 90 degrees clockwise on the flat surface of a semi-conductor wafer centering on a point 6. 2d of lower right semiconductor chip fields is the same pattern as the pattern made to rotate clockwise upper right semiconductor chip field 2c 90 degrees on the flat surface of a semi-conductor wafer centering on a point 6.

[0017] Lower left semiconductor chip field 2a has the pad 3 for a trial in the upper part of the right-hand side, and has a pad 5 to the field except the pad 3 for a trial on four sides. Upper left semiconductor chip field 2b has the pad 3 for a trial in the right part of the lower side, and has a pad 5 to the field except the pad 3 for a trial on four sides. Upper right semiconductor chip field 2c has the pad 3 for a trial in the lower part of left part, and has a pad 5 to the field except the pad 3 for a trial on four sides. 2d of lower right semiconductor chip fields has the pad 3 for a trial in the left part of a top chord, and they have a pad 5 to the field except the pad 3 for a trial on four sides.

[0018] Each semiconductor chip field 2a, 2b, and the pad 3 for a trial (2c and 2d) are concentrated and formed around a point 6, on it, arrange a probe card 4 and perform a semi-conductor wafer trial. The pad 3 for a trial contains a power-source pad, a grand pad, a clock pad, an input pad, and an output pad. The pad 3 for a trial is a pad it not only uses it at the time of normal operation, but used in a semi-conductor wafer trial.

[0019] In case a semi-conductor wafer trial is performed, the scanning (SCAN) design technique is used. The scanning design technique can examine normal or abnormalities, such as a component in a semiconductor chip field, or connection, without contacting a probe card needle only to the pad 3 for a trial, and contacting a probe card needle to a pad 5.

[0020] Drawing 3 shows four semiconductor chip field 2a which adjoins on a semi-conductor wafer, 2b, 2c, and the approach of measuring 2d simultaneously. A probe card 4 has the probe card needle 15 of the number of semiconductor chip field 2a and 2b of four pieces, and the pads 3 for a trial (2c and 2d), and the same number. The location of each needle of the probe card needle 15 is equivalent to the location of each pad of the pad 3 for a trial. Each needle of the probe card needle 15 is contacted to each pad of the pad 3 for a trial at coincidence, respectively, and semiconductor chip field 2a and 2b of four pieces, normal (2c and 2d), or abnormalities are examined simultaneously. Since 2d can be measured simultaneously, semi-conductor wafer test time can be shortened compared with semiconductor chip field 2a and 2b of four pieces, 2c, and the case where each semiconductor chip field is examined independently.

[0021] Drawing 4 shows the location of the pad 3 for a trial on semiconductor chip field 2a. The pad 3 for a trial contains the input pad and output pad other than the power-source pad VDD, the grand pad GND, and the clock pad CLK. For example, the grand pad GND is horizontally arranged at the location of L4 from the location of L1 (for example, 100 micrometers), and the right-hand side (an adjacent point 6 is included) from the top chord (an adjacent point 6 is included) of semiconductor chip field 2a to a perpendicular direction. The power-source pad VDD is horizontally arranged at the location of L4 from the location of L2 (for example, 200 micrometers), and the right-hand side (an adjacent point 6 is included) from the top chord (an adjacent point 6 is included) of semiconductor chip field 2a to a perpendicular direction. The clock pad CLK is horizontally arranged at the location of L4 from the location of L3 (for example, 300 micrometers), and the

right-hand side (an adjacent point 6 is included) from the top chord (an adjacent point 6 is included) of semiconductor chip field 2a to a perpendicular direction.

[0022] As mentioned above, regardless of the size of a semiconductor chip, the location of the pad 3 for a trial is considered as immobilization. Thereby, even if a chip size changes, it can examine using the same probe card 4. Furthermore, as for the pad 3 for a trial, it is desirable to specify sequence from a top like the order of the grand pad GND, the power-source pad VDD, and the clock pad CLK. However, if setting out of the circuit tester which will examine using a probe card 4 if the location of the pad for a trial is being fixed is changed even if it changes this sequence, it is possible to share the same probe card 4. In addition, semiconductor chip field 2b and 2c and 2d are the patterns same as mentioned above as the pattern made to rotate semiconductor chip field 2a, and the location of the pad 3 for a trial is fixed.

[0023] Drawing 5 shows the relation between a semi-conductor chip size and the location of the pad 3 for a trial. The semiconductor chip field unit 2 will change to the semiconductor chip field unit 11, if a semi-conductor chip size is made small, and if a semi-conductor chip size is enlarged, it will change to the semiconductor chip field unit 12. Even if a semi-conductor chip size changes, the location of each semiconductor chip field units 2 and 11 and the pad 3 for a trial in 12 is the same, and can share the same probe card 4.

[0024] (2nd operation gestalt) Drawing 6 is the top view of the semi-conductor wafer by the 2nd operation gestalt of this invention. Compared with the 1st operation gestalt, each semiconductor chip field 2a, 2b, and 2c and 2d have two pads 23a and 23b for a trial, and, as for this operation gestalt, it differs in that lower left semiconductor chip field 2a and upper right semiconductor chip field 2c are the same patterns, and are the pattern with 2 samed of upper left semiconductor chip field 2bs and lower right semiconductor chip fields.

[0025] It adjoins in order clockwise centering on an adjacent point 6 semiconductor chip field 2a, 2b, and 2c and 2d. Semiconductor chip field 2b and 2d are the same patterns as the pattern clockwise rotated 90 degrees on the flat surface of a semi-conductor wafer centering on the adjacent point 6 to semiconductor chip field 2a. Semiconductor chip field 2c is the same pattern as the pattern of semiconductor chip field 2a.

[0026] The semiconductor chip fields 2a and 2c have pad 23a for a trial in the upper part of the right-hand side, have pad 23b for a trial in the lower part of left part, and have a pad 25 to the field except the pads 23a and 23b for a trial on four sides. It has pad 23a for a trial in the right part of the lower side, has pad 23b for a trial in the left part of a top chord, and has semiconductor chip field 2b and 2d of pads 25 to the field except the pads 23a and 23b for a trial on four sides. These pads 23a and 23b for a trial are not twisted to a semi-conductor chip size, either, but it is fixed to the location where each pad was decided like drawing 4 .

[0027] The pad for a trial actually used for a semi-conductor wafer trial is explained. Pad 23for trial of semiconductor chip field 2a a, pad 23for trial a of semiconductor chip field 2b, pad 23for trial b of semiconductor chip field 2c, and pad 23b for the trial of 2d of semiconductor chip fields are concentrated and prepared around an adjacent point 6, are simultaneously contacted by the needle of a probe card 4, and can examine simultaneously semiconductor chip field 2a and 2b of four pieces, and normal or the abnormalities of 2c and 2d.

[0028] Other pads for a trial are explained. Although pad 23for trial b of semiconductor chip field 2a, pad 23for trial b of semiconductor chip field 2b, pad 23for trial a of semiconductor chip field 2c, and pad 23a for the trial of 2d of semiconductor chip fields are not used when performing a semi-conductor wafer trial by making the semiconductor chip field unit 2 into a unit, they can be used at the time of normal operation.

[0029] Also with the 2nd operation gestalt, since 2d can be measured simultaneously, semi-conductor wafer test time can be shortened compared with semiconductor chip field 2a and 2b of four pieces, 2c, and the case where each semiconductor chip field is examined independently. Moreover, since the location of the pads 23a and 23b for a trial in each semiconductor chip field is the same even if a semi-conductor chip size changes, the same probe card 4 can be shared.

[0030] (3rd operation gestalt) Drawing 7 is the top view of the semi-conductor wafer by the 3rd operation gestalt of this invention. Compared with the 1st operation gestalt, each semiconductor chip field 2a, 2b, and 2c and 2d have four pads 33a, 33b, 33c, and 33d for a trial, and, as for this operation gestalt, semiconductor chip field 2a and 2b of four pieces, and 2c differ from the point that 2d is the same pattern mutually.

[0031] Each semiconductor chip field 2a, 2b, and 2c and 2d, it has [ in the right part of pad 33for trial a, and the lower side ] pad 33d for a trial in the lower part of pad 33for trial b, and left part at the left part of pad 33for trial c, and a top chord at the upper part of the right-hand side, and has a pad 35 on four sides to the field except the pads 33a-33d for a trial. These pads 33a-33d for a trial are not twisted to a semi-conductor chip size, either, but it is fixed to the location where each pad was decided like drawing 4 .

[0032] The pad for a trial actually used for a semi-conductor wafer trial is explained. Pad 33for trial of semiconductor chip field 2a a, pad 33for trial b of semiconductor chip field 2b, pad 33for trial of semiconductor chip field 2c c, and pad 33d for the trial of 2d of semiconductor chip fields, it is prepared around an adjacent point 6 intensively, and is simultaneously contacted by the needle of a probe card 4, and semiconductor chip field 2a and 2b of four pieces, and normal or the abnormalities of 2c and 2d can be examined simultaneously.

[0033] Other pads for a trial are explained. Although the pads 33b, 33c, and 33d for a trial of semiconductor chip field 2a, the pads 33a, 33c, and 33d for a trial of semiconductor chip field 2b, the pads 33a, 33b, and 33d for a trial of semiconductor chip field 2c, and the pads 33a, 33b, and 33c for a trial of 2d of semiconductor chip fields are not used when performing a semi-conductor wafer trial by making the semiconductor chip field unit 2 into a unit, they can be used at the time of normal operation.

[0034] Also with the 3rd operation gestalt, since 2d can be measured simultaneously, semi-conductor wafer test time can be shortened compared with semiconductor chip field 2a and 2b of four pieces, 2c, and the case where each semiconductor chip field is examined independently. Moreover, since the pads [ in each semiconductor chip field / for a trial / 33a-33d ] location is the same even if a semi-conductor chip size changes, the same probe card 4 can be shared.

[0035] the 1- the inside of the side of four square shapes where two or more arrays of the semiconductor chip fields [ of four square shapes / four / which adjoined mutually on the semi-conductor wafer / 2a-2d ] group are carried out, and each semiconductor chip fields 2a-2d adjoin mutually, respectively as shown in the 3rd operation gestalt -- what is necessary is just to equip one of the sides with the bonding pad for a trial at least

[0036] (4th operation gestalt) Drawing 8 is the top view of the semi-conductor wafer by the 4th operation gestalt of this invention. this operation gestalt -- the 1- compared with the 3rd operation gestalt, it differs in that the semiconductor chip fields 42a, 42b, and 42c of three square shapes [ forward six ] adjoin mutually on a semi-conductor wafer.

[0037] Each semiconductor chip fields 42a, 42b, and 42c have the pad 43 for a trial around the point 46 that the semiconductor chip fields 42a-42c touch mutually, respectively. The pad 43 for a trial of the semiconductor chip fields 42a-42c is concentrated and formed around an adjacent point 46, is simultaneously

contacted by the needle of a probe card 44, and can examine simultaneously normal or the abnormalities of three semiconductor chip fields 42a-42c. This pad 43 for a trial is not twisted to a semi-conductor chip size, either, but it is fixed to the location where each pad was decided.

[0038] With the 4th operation gestalt, since three semiconductor chip fields 42a-42c can be measured simultaneously, semi-conductor wafer test time can be shortened compared with the case where each semiconductor chip field is examined independently. Moreover, since the location of the pad 43 for a trial in a semiconductor chip field is the same even if a semi-conductor chip size changes, the same probe card 44 can be shared.

[0039] As shown in the 4th operation gestalt, two or more arrays of the group of the semiconductor chip fields 42a-42c of three square shapes [ six ] which adjoined mutually on the semi-conductor wafer are carried out, and inside [ each semiconductor chip fields 42a-42c are the sides of six square shapes which adjoin mutually, respectively ] should just equip one of the sides with the pad 43 for a trial at least.

[0040] In recent years, especially in the system ASIC, want of a short delivery date has become strong, and turn around time is becoming short by improvement in a semi-conductor design and a process technique. Conventionally, whenever the semi-conductor chip size changed, the probe card newly had to be created, and the delay of a delivery date had arisen.

[0041] the 1- even when according to the 4th operation gestalt the semiconductor chip field of a multipolygon concentrates and arranges the pad for a trial of each semiconductor chip field near the central point which adjoins mutually and the size of a semiconductor chip changes, it becomes possible to arrange the bonding pad for a trial in the same location. If the location of BONTINGUPADDO for a trial is decided without depending on the size of a semiconductor chip, it becomes unnecessary to be able to share the probe card same at the time of a semi-conductor wafer trial, and to newly create a probe card, and reduction-ization of cost can be attained in the production time of a semiconductor chip, and the shortening list of a delivery date.

[0042] Moreover, since the semiconductor chip field unit which consists of a group of three pieces or four semiconductor chip fields, for example can be measured simultaneously, semi-conductor wafer test time can be shortened compared with the case where each semiconductor chip field is examined independently. Two or more arrays of the semiconductor chip field unit are carried out on the semi-conductor wafer. In a semi-conductor wafer trial, it can examine by moving a probe card for every semiconductor chip field unit.

[0043] In addition, it passes over no above-mentioned operation gestalten to what showed a mere example of the somatization which hits carrying out this invention, and the technical range of this invention must not be restrictively interpreted by these. That is, this invention can be carried out in various forms, without deviating from the pneuma or its main description.

[0044] It is as follows when various gestalten of this invention are summarized.

(Additional remark 1) It is the semi-conductor wafer characterized by the thing of the sides which it is the semi-conductor wafer which has the group of the semiconductor chip field of the multipolygon which adjoins mutually, and each semiconductor chip field adjoins mutually within the group of said semiconductor chip field, respectively for which one of the sides was equipped with the bonding pad for a trial at least.

(Additional remark 2) Each semiconductor chip field is the semi-conductor wafer of the additional remark 1 publication characterized by the thing of the sides of said polygon which adjoins mutually for which one of the sides was equipped with the bonding pad for a trial at least, respectively including the semiconductor chip field of the polygon of four pieces where said semi-conductor wafer adjoined mutually.

[0045] (Additional remark 3) Each semiconductor chip field is the semi-conductor wafer of the additional remark 2 publication characterized by the thing of the sides of said four square shapes which adjoin mutually for which one of the sides was equipped with the bonding pad for a trial at least, respectively including the semiconductor chip field of four square shapes [ four ] where said semi-conductor wafer adjoined mutually.

(Additional remark 4) The group of the semiconductor chip field of four square shapes [ four ] where said semi-conductor wafer adjoined mutually is the semi-conductor wafer of additional remark 3 publication with which two or more arrays are carried out, and each semiconductor chip field is characterized by the thing of the sides of said four square shapes which adjoin mutually for which one of the sides was equipped with the bonding pad for a trial at least, respectively.

[0046] (Additional remark 5) the semiconductor chip field of said four square shapes [ four ] -- this -- the semi-conductor wafer of the additional remark 4 publication characterized by being the same pattern as the pattern each other rotated by a unit of 90 degrees on the flat surface of said semi-conductor wafer centering on the point that four semiconductor chip fields touch mutually, respectively.

(Additional remark 6) The semiconductor chip field of said four square shapes [ four ] The 1st, 2nd, 3rd, and 4th semiconductor chip fields adjoin mutually clockwise. Said 2nd and 4th semiconductor chip fields It is the same pattern as the pattern rotated 90 degrees on the flat surface of said semi-conductor wafer centering on the point that the 4th semiconductor chip field touches mutually. said 1st semiconductor chip field -- receiving -- respectively -- said the 1- Said 3rd semiconductor chip field is the semi-conductor wafer of the additional remark 4 publication characterized by being the same pattern as the pattern of said 1st semiconductor chip field.

[0047] (Additional remark 7) the semiconductor chip field of said four square shapes [ four ] -- clockwise -- the 1st, 2nd, 3rd, and 4th semiconductor chip fields -- mutual -- adjoining -- **** -- said the 1- the semi-conductor wafer of the additional remark 4 publication characterized by the 4th semiconductor chip field being the same pattern mutually.

(Additional remark 8) Said bonding pad for a trial is the semi-conductor wafer of the additional remark 4 publication characterized by including a power-source bonding pad, a grand bonding pad, a clock bonding pad, an input bonding pad, and an output bonding pad.

[0048] (Additional remark 9) Each semiconductor chip field is the semi-conductor wafer of the additional remark 1 publication characterized by the thing of the sides of said polygon which adjoins mutually for which one of the sides was equipped with the bonding pad for a trial at least, respectively including the semiconductor chip field of the polygon of three pieces where said semi-conductor wafer adjoined mutually.

(Additional remark 10) Each semiconductor chip field is the semi-conductor wafer of the additional remark 9 publication characterized by the thing of the sides of said six square shapes which adjoin mutually for which one of the sides was equipped with the bonding pad for a trial at least, respectively including the semiconductor chip field of three square shapes [ six ] where said semi-conductor wafer adjoined mutually.

[0049] (Additional remark 11) The group of the semiconductor chip field of three square shapes [ six ] where said semi-conductor wafer adjoined mutually is the semi-conductor wafer of additional remark 10 publication with which two or more arrays are carried out, and each semiconductor chip field is characterized by the thing of the sides of said six square shapes which adjoin mutually for which one of the sides was equipped with the bonding pad for a trial at least, respectively.

It is the semi-conductor wafer which has the group of the semiconductor chip field of the

multipolygon which adjoins mutually. (Additional remark 12) Each semiconductor chip field is the test method of the semi-conductor wafer of the sides which adjoin mutually within the group of said semiconductor chip field, respectively which equipped one of the sides with the bonding pad for a trial at least. The test method of the semi-conductor wafer which a probe card needle is simultaneously contacted to the bonding pad for a trial of two or more of said semiconductor chip fields which adjoin mutually, and examines simultaneously two or more of said normal or abnormalities of a semiconductor chip field which adjoin mutually.

[0050] Said semi-conductor wafer includes the semiconductor chip field of the polygon of four pieces which adjoined mutually. (Additional remark 13) Each semiconductor chip field It is the test method of the semi-conductor wafer of the sides of said polygon which adjoins mutually which equipped one of the sides with the bonding pad for a trial at least, respectively. The test method of the semi-conductor wafer of the additional remark 12 publication which a probe card needle is simultaneously contacted to the bonding pad for a trial of said four semiconductor chip fields which adjoin mutually, and examines simultaneously said normal or abnormalities of four semiconductor chip fields which adjoin mutually.

Said semi-conductor wafer includes the semiconductor chip field of four square shapes [ four ] which adjoined mutually. (Additional remark 14) Each semiconductor chip field It is the test method of the semi-conductor wafer of the sides of said four square shapes which adjoin mutually which equipped one of the sides with the bonding pad for a trial at least, respectively. The test method of the semi-conductor wafer of the additional remark 13 publication which a probe card needle is simultaneously contacted to the bonding pad for a trial of said four semiconductor chip fields which adjoin mutually, and examines simultaneously said normal or abnormalities of four semiconductor chip fields which adjoin mutually.

[0051] Two or more arrays of the group of the semiconductor chip field of four square shapes [ four ] where said semi-conductor wafer adjoined mutually are carried out. (Additional remark 15) Each semiconductor chip field It is the test method of the semi-conductor wafer of the sides of said four square shapes which adjoin mutually which equipped one of the sides with the bonding pad for a trial at least, respectively. The test method of the semi-conductor wafer of the additional remark 14 publication which a probe card needle is simultaneously contacted to the bonding pad for a trial of said four semiconductor chip fields which adjoin mutually, and examines simultaneously said normal or abnormalities of four semiconductor chip fields which adjoin mutually.

(Additional remark 16) The semiconductor chip field of said four square shapes [ four ] It is the test method of the semi-conductor wafer which is the same pattern as the pattern each other rotated by a unit of 90 degrees on the flat surface of said semi-conductor wafer, respectively centering on the point that the semiconductor chip field of these four individuals touches mutually. The test method of the semi-conductor wafer of the additional remark 15 publication which a probe card needle is simultaneously contacted to the bonding pad for a trial of said four semiconductor chip fields which adjoin mutually, and examines simultaneously said normal or abnormalities of four semiconductor chip fields which adjoin mutually.

[0052] (Additional remark 17) The semiconductor chip field of said four square shapes [ four ] The 1st, 2nd, 3rd, and 4th semiconductor chip fields adjoin mutually clockwise. Said 2nd and 4th semiconductor chip fields It is the same pattern as the pattern rotated 90 degrees on the flat surface of said semi-conductor wafer centering on the point that the 4th semiconductor chip field touches mutually. said 1st semiconductor chip field -- receiving -- respectively -- said the 1- Said 3rd semiconductor chip field is the test method of the semi-conductor wafer which is the same pattern as the pattern of said 1st semiconductor chip field. The test method of the semi-conductor wafer of the additional remark 15 publication which a probe card needle is

simultaneously contacted to the bonding pad for a trial of said four semiconductor chip fields which adjoin mutually, and examines simultaneously said normal or abnormalities of four semiconductor chip fields which adjoin mutually.

(Additional remark 18) The semiconductor chip field of said four square shapes [ four ] clockwise -- the 1st, 2nd, 3rd, and 4th semiconductor chip fields -- mutual -- adjoining -- **** -- said the 1- the 4th semiconductor chip field Are the test method of the semi-conductor wafer which is the same pattern mutually, and a probe card needle is simultaneously contacted to the bonding pad for a trial of said four semiconductor chip fields which adjoin mutually. The test method of the semi-conductor wafer of the additional remark 15 publication which examines simultaneously said normal or abnormalities of four semiconductor chip fields which adjoin mutually.

[0053] (Additional remark 19) Said bonding pad for a trial is the semi-conductor wafer of the additional remark 15 publication characterized by including a power-source bonding pad, a grand bonding pad, a clock bonding pad, an input bonding pad, and an output bonding pad.

Said semi-conductor wafer includes the semiconductor chip field of the polygon of three pieces which adjoined mutually. (Additional remark 20) Each semiconductor chip field It is the test method of the semi-conductor wafer of the sides of said polygon which adjoins mutually which equipped one of the sides with the bonding pad for a trial at least, respectively. The test method of the semi-conductor wafer of the additional remark 12 publication which a probe card needle is simultaneously contacted to the bonding pad for a trial of said three semiconductor chip fields which adjoin mutually, and examines simultaneously said normal or abnormalities of three semiconductor chip fields which adjoin mutually.

[0054] Said semi-conductor wafer includes the semiconductor chip field of three square shapes [ six ] which adjoined mutually. (Additional remark 21) Each semiconductor chip field It is the test method of the semi-conductor wafer of the sides of said six square shapes which adjoin mutually which equipped one of the sides with the bonding pad for a trial at least, respectively. The test method of the semi-conductor wafer of the additional remark 20 publication which a probe card needle is simultaneously contacted to the bonding pad for a trial of said three semiconductor chip fields which adjoin mutually, and examines simultaneously said normal or abnormalities of three semiconductor chip fields which adjoin mutually. Two or more arrays of the group of the semiconductor chip field of three square shapes [ six ] where said semi-conductor wafer adjoined mutually are carried out. (Additional remark 22) Each semiconductor chip field It is the test method of the semi-conductor wafer of the sides of said six square shapes which adjoin mutually which equipped one of the sides with the bonding pad for a trial at least, respectively. The test method of the semi-conductor wafer of the additional remark 21 publication which a probe card needle is simultaneously contacted to the bonding pad for a trial of said three semiconductor chip fields which adjoin mutually, and examines simultaneously said normal or abnormalities of three semiconductor chip fields which adjoin mutually.

[0055]

[Effect of the Invention] As explained above, even when the size of a semiconductor chip changes according to this invention, it becomes possible to arrange the bonding pad for a trial in a semiconductor chip field in the same location. If the location of BONTINGUPADDO for a trial is decided without depending on the size of a semiconductor chip, it becomes unnecessary to be able to share the probe card same at the time of a semi-conductor wafer trial, and to newly create a probe card, and reduction-ization of cost can be attained in the production time of a semiconductor chip, and the shortening list of a delivery date.

[0056] Moreover, a probe card needle can be simultaneously contacted to the bonding pad for a trial

of two or more semiconductor chip fields which adjoin mutually, and semi-conductor wafer test time can be shortened compared with normal or the case where each semiconductor chip field is independently examined since abnormalities can be examined simultaneously of two or more semiconductor chip fields which adjoin mutually.

[Brief Description of the Drawings]

[Drawing 1] It is the top view of the semiconductor chip field on the semi-conductor wafer by the 1st operation gestalt of this invention.

[Drawing 2] It is the top view of the whole semi-conductor wafer.

[Drawing 3] It is the top view of a semiconductor chip field showing the coincidence measurement in a semi-conductor wafer trial.

[Drawing 4] It is the top view showing some pads for a trial in a semiconductor chip field.

[Drawing 5] It is the top view of a semiconductor chip field when a semi-conductor chip size changes.

[Drawing 6] It is the top view of the semiconductor chip field on the semi-conductor wafer by the 2nd operation gestalt of this invention.

[Drawing 7] It is the top view of the semiconductor chip field on the semi-conductor wafer by the 3rd operation gestalt of this invention.

[Drawing 8] It is the top view of the semiconductor chip field on the semi-conductor wafer by the 4th operation gestalt of this invention.

[Drawing 9] It is the top view of a semiconductor chip field showing the semi-conductor wafer trial by the conventional technique.

[Drawing 10] It is the top view of a semiconductor chip field showing the coincidence measurement in a semi-conductor wafer trial.

[Description of Notations]

1 Semi-conductor Wafer

2 Semiconductor Chip Field Unit

2a, 2b, 2c, 2d Semiconductor chip field

3 Pad for Trial

4 Probe Card

5 Pad

6 Adjacent Point

11 12 Semiconductor chip field

15 Probe Card Needle

23a, 23b Pad for a trial

25 Pad

33a-33d Pad for a trial

35 Pad

42a-42c Semiconductor chip field

43 Pad for Trial

44 Probe Card

52 Semiconductor Chip Field

54 Probe Card

55 Pad

56 Probe Card Needle

57 Power-Source Pad

62 Semiconductor Chip Field

63 Pad for Trial

64 Probe Card

65 Pad

66 Probe Card Needle